Zalt Z80 Computer

A retro computer with modern hardware.

A journey of learning.

# Design

There are three main components:

1. Computation  
   The Z80 CPU and the core Memory.
2. The System Controller  
   Orchestrates system functions such as boot and IO.
3. The System Logic  
   All glue logic is located here. Everything is connected using buses.

## Computation

### CPU

Z80

### Memory

Bank switched memory to rise above the 64k limit. MA12-MA19 (1MB) MBE1-MBE7 (64k banks).

No ROM, RAM only. Need System Controller to load in BIOS (shadow ROM).

### System Bus

CPU bus

Extend Memory Addresses

## System Controller

Atmel ATmega128A -or-

Cypress PSoC 5LP

### Reading and Writing Memory over the System Bus (BUSREQ/DMA)

The System Controller takes control over the System Bus using the Z80 BUSREQ/BUSACK handshake.  
The System Controller reads or writes to the Memory directly (DMA). The Memory Controller (System Logic) is active to translate internal bus addresses into memory banked addresses.

### System Controller Register Access by CPU over the System Bus (IOREQ)

The CPU performs an In/Out instruction (IOREQ) to read or write the System Controller registers. The System Logic performs the address decoding for the range of IO addresses targeted at the System Controller. When it is detected the System Controller’s IO address range is targeted, it receives and signal from the System Logic. The RD and WR (together with the IOREQ) signals indicate if data is read or written.

We (may) need extra Wait-States for the slow(er) System Controller to have enough time to provide the data for IO-Input.

### External Input / Output

SPI/I2C/UART

## System Logic

Altera Max II  
3.3V so need level shifters (passives).

### Clock Controller

Divides central clock (50MHz) into clocks for System Controller (16MHz) and a programmable CPU clock – for debug purposes.

Single Step CPU clock (instruction based –M1?)

## Memory Controller

Built with discreet logic – not part of the System-Logic component.

Uses a fast cache SRAM to do the translation. Need latches for programming table content.

Always on: translates A12-A15 with the Bank Switch Registers to MA12-MA19.

Also works for System Controller access.

## External Bus

Interfacing with core.

2x 40 pin header connector (IDC).

Connector 1: basic memory bus with Address and Data bus plus control lines as MEMREQ and RD/WR.   
Connector 2: IO bus with extra decoded enable signals and IOREQ, WAIT, HALT etc.

### Extension Bus

Modular design.

### Serial UART

Currently main I/O – text and commands.

### Debug Serial

Private Debug channel

### I2C

System extension

### Input Devices

Keyboard / Mouse